Brunswick

SERVICE BULLETIN

Capital Equipment Division

Subject: I/O PCB Jumper Settings Date: 10/1/01

Distribution: Selected Frameworx Scorer Customers Letter No. CEB01-7

It has come to our attention that some of the newer style I/O PCBs located in the Lane Group Processor (LGP) may have been installed with their on-board jumpers set incorrectly. Although the LGP may function without problems, the improper settings may cause occasional scorer lockups. Page 2 of this bulletin describes the function and configuration for the jumpers and switches on the new I/O PCB.

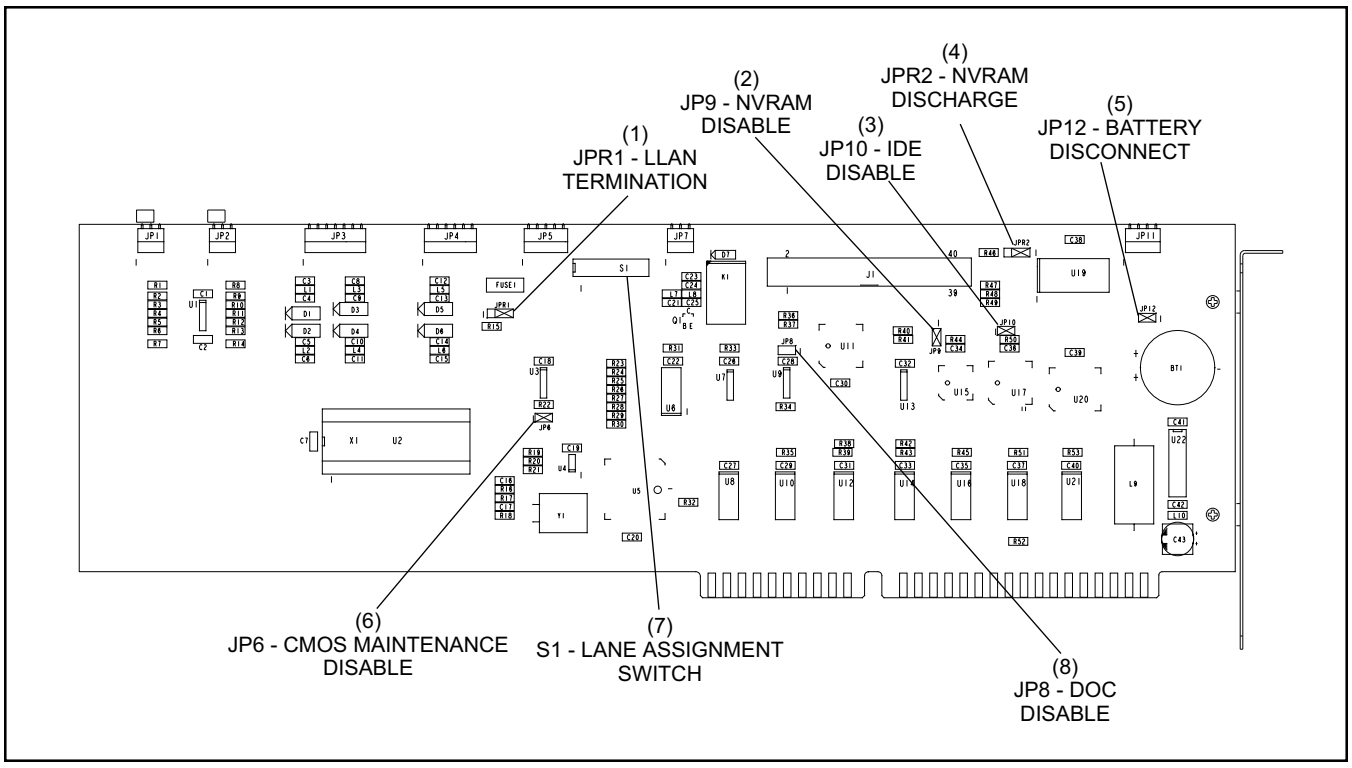
If your center uses this type of LGP I/O PCB, please **verify the placement of all jumpers. All should be set using the default settings shown on page 2.**

If you have any questions regarding the configuration, please contact Brunswick's Customer Response Center at 1-800-323-8141.

Bill Jager
Service Product Engineer

David E. Rice
Director of Training and Support

I/O PCB - B Jumper Settings



I/O PCB - B

(1) <u>JPR1: LLAN Termination</u>

Pins 1-2 = Terminated
Pins 2-3 = Unterminated (Default)

(2) <u>JP9: NVRAM Disable</u>

Installed = NVRAM Enabled (Default)
Not Installed = NVRAM Disabled

(3) <u>JP10: IDE Disable</u>

Installed = IDE Enabled (Default)
Not Installed = IDE Disabled

(4) <u>JPR2: NVRAM Discharge</u>

Pins 1-2 = Do not Discharge (Default)
Pins 2-3 = Discharge

(5) <u>JP12: Battery Disconnect</u>

Installed = On board battery connected (Default)
Not installed = On board battery disconnected

(6) <u>JP6: CMOS Maintenance Disable</u>

Installed = CMOS Maintenance Enabled (Default)
Not Installed = CMOS Maintenance Disabled

(7) <u>S1: Lane Assignment Switches</u>

Set switches to equal left lane number

Switch On = Value Enabled
Switch Off = Value Disabled

Switch #	Value
1	1
2	2
3	4
4	8
5	16
6	32
7	64
8	128

(8) <u>JP8: DOC (Disk on Chip) Disable</u>

Installed = DOC Enabled
Not Installed = DOC Disabled (Default)